

# ECE2031 In-Class Exam Spring 2007

## ANSWER SHEET

Name \_\_\_\_\_ Section \_\_\_\_\_ Student No. \_\_\_\_\_

Closed Books, Closed Notes, No computers or calculators.

Having read the Georgia Institute of Technology Academic Honor Code, I understand and accept my responsibility as a member of the Georgia Tech Community to uphold the Honor Code at all times. In addition, I understand my options for reporting honor violations as detailed in the code.

\_\_\_\_\_  
(Signature)

\_\_\_\_\_  
(Date)

CIRCLE YOUR SELECTED ANSWERS OR FILL IN AS NEEDED

1. a b c d e (5 pts)
2. a b c d e (5 pts)
3. a b c d e (5 pts)
4. a b c d e (5 pts)
5. a b c (5 pts)
6. a b c d e (5 pts)
7. (15 pts)

CD \ AB	00	01	11	10
00				
01				
11				
10				

Y= \_\_\_\_\_

(When writing your equation, be careful to separate any bars that you intend to be interpreted as separated:  $\overline{XY}$  as opposed to  $\overline{X} \overline{Y}$ )

Questions 8-14: Write ONE letter in the range of “a” through “k” in each blank.

- 8. \_\_\_\_ (2 pts)
- 9. \_\_\_\_ (2 pts)
- 10. \_\_\_\_ (2 pts)
- 11. \_\_\_\_ (2 pts)
- 12. \_\_\_\_ (2 pts)
- 13. \_\_\_\_ (2 pts)
- 14. \_\_\_\_ (2 pts)
- 15. a b (4 pts)
- 16. a b c (4 pts)
- 17. a b (4 pts)
- 18. a b (4 pts)

19. Fill in the Next State and Z columns. The first row is filled in correctly as an example (15 pts)

Present State	X <sub>1</sub>	X <sub>0</sub>	Next State	Z
A	0	0	A	0
A	0	1		
A	1	0		
A	1	1		
B	0	0		
B	0	1		
B	1	0		
B	1	1		
C	0	0		
C	0	1		
C	1	0		
C	1	1		
D	0	0		
D	0	1		
D	1	0		
D	1	1		

- 20. a b c d e (5 pts)
- 21. a b c d e (5 pts)

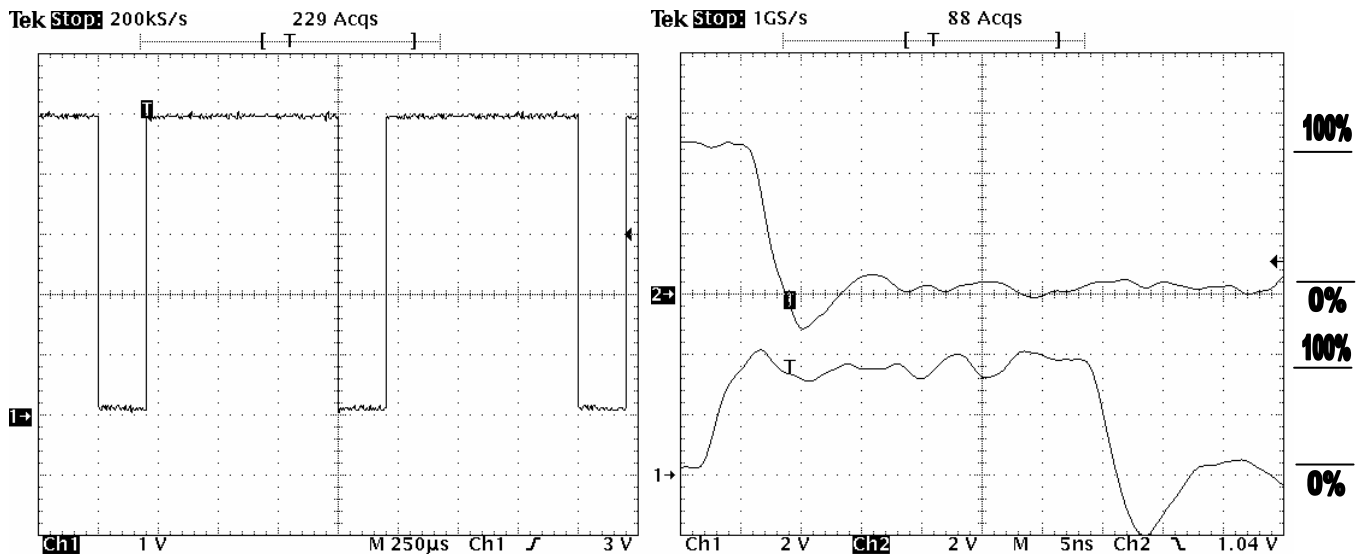
NAME: \_\_\_\_\_

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Mark all answers on the answer sheet, but turn these pages in, too.**

**Questions 1-3:** The images below show two different signal acquisitions. There is no relation between them, and the respective scales are shown for both time and voltage. You may assume that when the signals *appear* to repeat, they *do* repeat. These do not necessarily show optimal placement and scaling, but they are adequate for the resolution requested for the problems.

FOR THE SIGNALS ON THE RIGHT, there is large overshoot, and you do not have sufficient data to tell where the 0% and 100% levels are (if the signals were allowed to settle). So assume that for the top right waveform, 0% is 0.4V and 100% is 4.8V, approximately where the percentage markers are shown. And for the bottom right waveform, 0% is also 0.4 V, but 100% is 3.6 V.

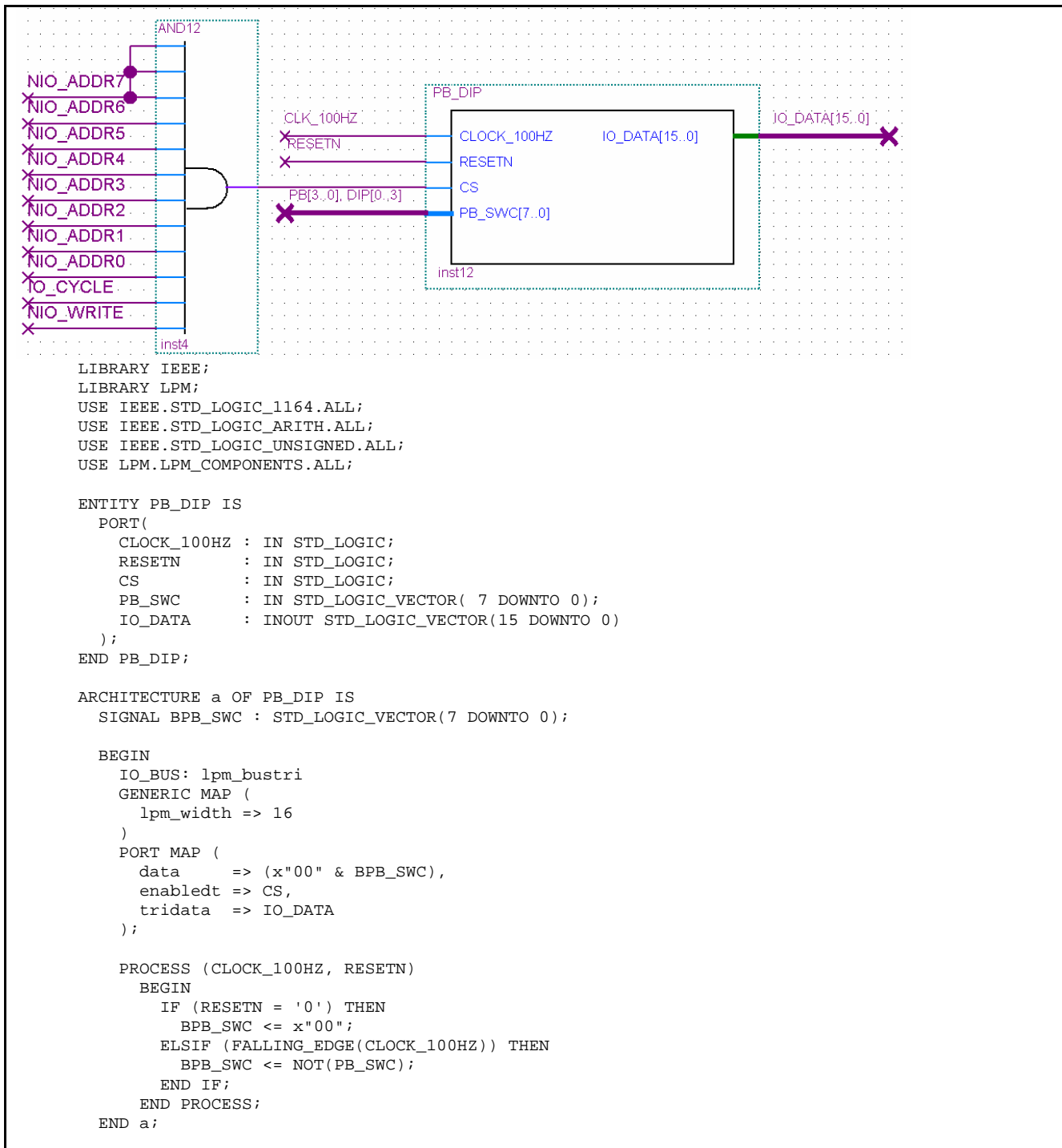


From these figures, estimate the following parameters:

1. (5 pts) Left Figure: Positive duty cycle of the waveform
  - a) 800 µs
  - b) 0.8%
  - c) 80%
  - d) 20%
  - e) 2 ns
  
2. (5 pts) Right Figure: Fall time of the lower waveform (channel 1)
  - a) ~1.5 ns
  - b) ~2 ms
  - c) ~5 ns
  - d) ~9 ns
  - e) ~30ns
  
3. (5 pts) Right Figure: Propagation delay from the rising edge of channel 1 (the lower signal) to the falling edge of channel 2 (the upper signal)
  - a) 0.8 ns
  - b) 4 ns
  - c) 11 ns
  - d) 2 V
  - e) 29 ns

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The following shows both the symbol and the VHDL source for PB\_DIP, exactly as it appears in the downloadable *top\_scomp* project that is the starting point for the final design project. The AND gate that drives CS is also shown. Questions 4, 5, and 6 refer to this information.



4. (5 pts) When CS is asserted (high), and RESETN is not asserted (i.e., RESETN is also high), what is the best description of what happens on the lower 8 bits of IO\_DATA?

- a) They are held in the tristate condition
- b) They show the current value of the switches
- c) They show the inverted value of the switches, as sampled within the last 0.01 sec
- d) They show the inverted, current value of the switches
- e) They show the value x"00"

NAME: \_\_\_\_\_

5. (5 pts) Still referring to the preceding figure and code, IO\_BUS represents a device, and the PROCESS statement represents a device. These two devices are operating

- a) in parallel (concurrently)
- b) sequentially
- c) neither of the above

6. (5 pts) Still referring to the preceding figure and code, and assuming that NIO\_ADDRn is NOT(IO\_ADDRn) and NIO\_WRITE is NOT(IO\_WRITE), what does the 12-input AND do?

- a) Decodes an I/O address of 0x00, when IO\_CYCLE is high and IO\_WRITE is low
- b) Decodes an I/O address of 0xFF, when IO\_CYCLE is high and IO\_WRITE is low
- c) Decodes an I/O address of 0x00, when IO\_CYCLE is low and IO\_WRITE is high
- d) Decodes an I/O address of 0xFF, when IO\_CYCLE is low and IO\_WRITE is high
- e) Decodes an I/O address of 0xFF, when IO\_CYCLE is high and IO\_WRITE is high

7. (15 points) Fill in the Karnaugh Map for the following truth table and solve it, circling the prime implicants and writing the minimal sum of products expression.

ABCD	Y
0000	1
0001	1
0010	0
0011	1
0100	1
0101	1
0110	0
0111	0
1000	0
1001	1
1010	0
1011	1
1100	0
1101	0
1110	1
1111	0

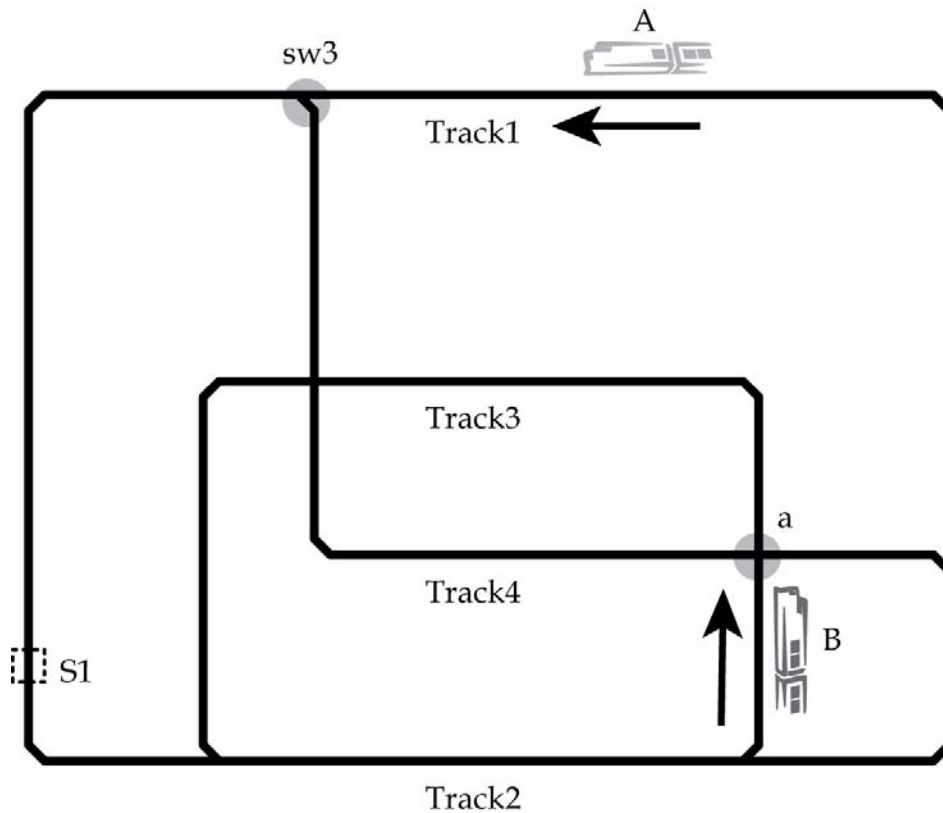
**Questions 8-14** (2 pts each): Fill in the blanks in the following paragraph by selecting a choice from the list below for each numbered blank. For example, if you think the first blank should be filled in with “EPC6”, enter the letter “h” for question 8. (Not all list items will be used.)

\_\_\_\_(8)\_\_\_\_ language code is assembled by \_\_\_\_ (9) \_\_\_\_, producing \_\_\_\_ (10) \_\_\_\_ language code that is directly stored in a instance of the \_\_\_\_ (11) \_\_\_\_ Megafunction. The memory code is combined with FPGA \_\_\_\_ (12) \_\_\_\_ information in a(n) \_\_\_\_ (13) \_\_\_\_ file that is downloaded to the Cyclone chip by the Quartus \_\_\_\_ (14) \_\_\_\_ tool.

- a) sof
- b) mif
- c) SCASM
- d) machine
- e) programming
- f) assembly
- g) SCOMP
- h) EPC6
- i) altsyncram
- j) configuration
- k) simulator

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**Questions 15-18** refer to the following train situation. Not all switches and sensors are shown, but you may assume that this is EXACTLY the same setup of switches, sensors, tracks, and power supplies that you used in Lab 6. At this instant, the trains are moving in the direction shown by the arrows.



15. (4 points) There is a switch at the point labeled “a” that determines whether train B will stay on Track 3 or switch to Track 4.
- a) TRUE
  - b) FALSE
16. (4 points) In order to avoid a crash or derailment, the controller at this particular state should have switch sw3 . . .
- a) set such that it is connected straight through (Track1 to Track1)
  - b) set such that it connects Track4 to Track1
  - c) set either way, because it does not matter as long as Train A is where it is now shown
17. (4 points) Sensor S1 is high (1) at this instant.
- a) TRUE
  - b) FALSE
18. (4 points) It is possible that trains A and B are driven by the same power supply at this instant.
- a) TRUE
  - b) FALSE



NAME: \_\_\_\_\_

For the next two questions, consider the following ASM code. Assume this has been assembled and run on SCOMP. Reminder: the SHIFT instruction shifts left if the operand is positive, and right if the operand is negative.

```
                ORG      &H000    ;Begin program at x000

Start:  LOAD      A
        SHIFT    15
        JNEG     Neg
        LOAD     PosSig
        JUMP     Next
Neg:    LOAD     NegSig
Next:   STORE    B
        LOAD     ZERO
        JZERO   Done
        LOAD     C
Done:   JUMP     Done

A:      DW       &H0001
B:      DW       &H0002
C:      DW       &H000C
PosSig: DW       &H000F
NegSig: DW       &HFFFF
ZERO:   EQU     &H0000
```

20. (5 points) What is stored in location “B” at the end of program (i.e., after it starts looping forever at “Done”)?

- a) &H0002
- b) &H000F
- c) &HFFFF
- d) &H0000
- e) Impossible to tell from the information given

21. (5 points) Also at the end of the program, what is the value of the accumulator (AC)?

- a) &H0000
- b) &H0002
- c) &H000C
- d) Impossible to tell from the information given
- e) None of the above (the value can be determined, but it is not a, b, or c)