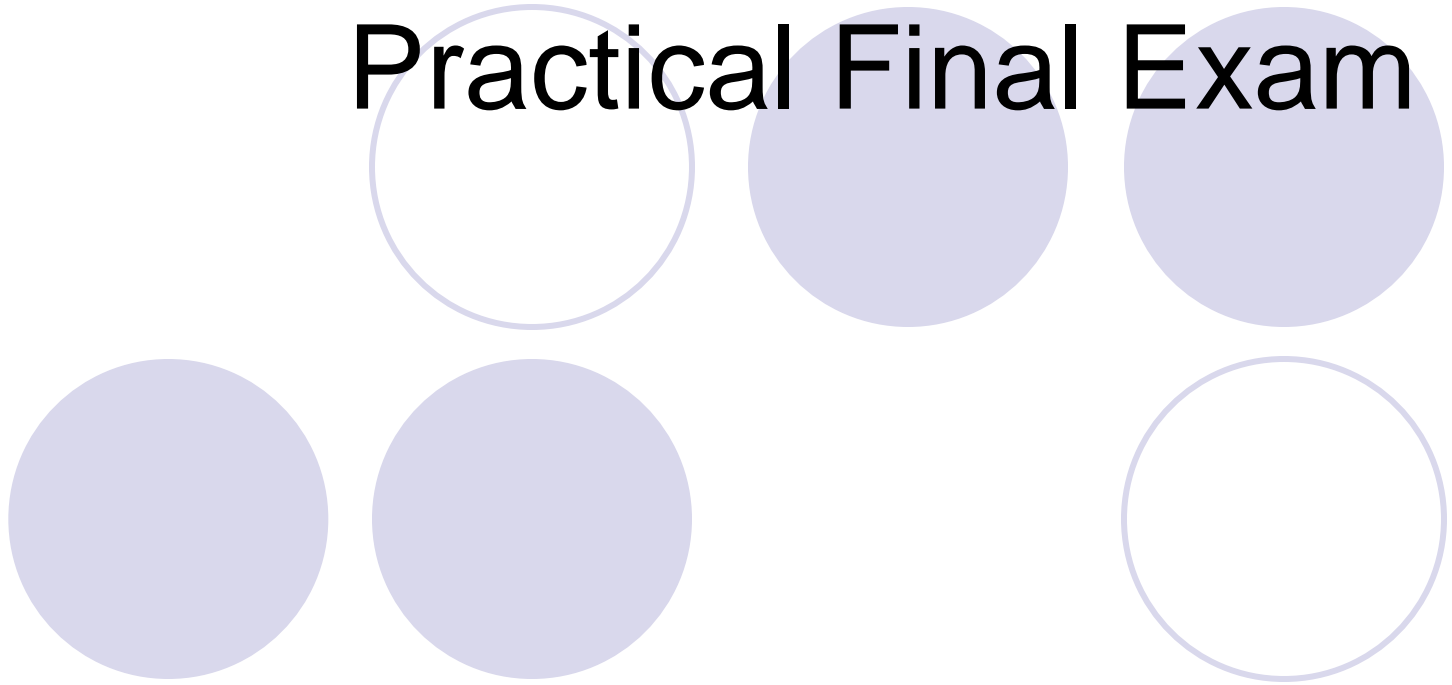


Review for Practical Final Exam



Announcements



- Practical Exam Tuesday-Thursday (Nov. 10-12) IN LAB (your scheduled time)
- ~2 weeks of project work, then Holiday and Final Demos
- Use last day (Nov. 30) for nothing more than fine-tuning
 - If 30 teams are trying to complete their demo on the last day, most will be unfinished

Practical Final exam

- Will be held IN YOUR REGULAR LAB SESSION
- No make-ups except in those same severe conditions that the Institute would consider as valid for any other final exam
- There is NO exam for this course during finals week
- Approximately ~~2.5~~ **Exactly 2.0** hours of “practical” exercises (working with lab tools, both hardware and software)
 - You must start on time if you want all the time

Practical Exam Procedures



- Open book, open notes
 - You'll do better if you don't have to hunt for answers
- TAs cannot assist you with basic skills, setup, etc.
- You cannot access your own home directory, Internet, flash drives, floppy disks, or other media (No ftp, http file transfers)
- Each answer gets checked off by TA
 - Full credit if correct on first checkoff attempt
 - Half credit if correct on second checkoff attempt
- Move on after two attempts
- No requirement to go in order. Plan your own time.

Practical Exam Content



- Probably about ~~5-6~~ ⁴⁻⁵ numbered problems, some with multiple parts
 - A problem may have multiple parts with some interdependence, but a numbered problem will not depend on a previous one.
- Most emphasize one or more aspects of the design tools (Block Editor, VHDL compiler, Timing Analyzer, Waveform editor/Simulator, Oscilloscope, ~~Logic Analyzer~~, etc.)
- No need to bring chips or protoboard or wire kit.
- Some exercises require oscilloscope measurements
 - You must connect probes to the expansion header of the DE2 board, similar to Lab 3

Practical Exam: You Should Know How To ...

- Use Quartus tools, including
 - Schematic entry,
 - VHDL entry,
 - Waveform Editor/Simulation,
 - Pin Planner (and device assignment),
 - Compilation,
 - Interpret Compilation Report (incl. Timing Analysis),
 - Programming (downloading)

Practical Exam: You Should Know How To ...

- Use a part from Altera library
 - create from MegaWizard, where applicable
 - understand its help information, etc.
- Find things on the DE2 board
 - Where Cyclone pins go to headers, switches, etc.
 - USB-Blaster connector, VGA connector, etc.
- Download sof files to the DE2 board

Practical Exam: You Should Know How To ...

- Write/understand VHDL
 - Write the VHDL code to synthesize a given word description or circuit
 - VHDL coding could be “from scratch” on practical final exam

Practical Exam: You Should Know How To ...

- Work with state machines
 - Generate an ASM chart for a state machine from a word description
 - Generate the VHDL CASE statement to synthesize a state machine from an ASM chart
 - Recognize bugs in implemented VHDL state machines, when compared with the corresponding state diagram
 - Work with state machine examples like simple versions of the train controller

Practical Exam: You Should Know How To ...

- **Alter SCOMP**

- Implement new instructions
- Work with I/O devices (old or new)
- Find bugs

- **Program SCOMP**

- Write short programs
- Use SCASM to assemble
- Verify operation
- I/O-related problems?

Practical Exam: You Should Know How To ...

- Use Oscilloscope

- Use the oscilloscope to perform basic measurements of signals (propagation delay, rise/fall time, duty cycle, period, frequency, etc.)
- Be able to capture a trace that clearly shows these values, with appropriate time scale and voltage scale

How to prepare



- If you understood what you were doing in each lab, and still remember, you are probably prepared
- If you did poorly on a lab, or managed a good grade on something that didn't really make sense, you should consider going through it again
- Exercises will not be the same as labs, but the tasks are similar

Interested in being a UTA?



- See http://diglab.ece.gatech.edu/ta_FAQ.html
- **Benefits**
 - 1 hour general credit
 - Looks good on your resume
 - Prerequisite for being a Lead TA (a paid position)
 - Good preparation for being a GTA (if you are considering graduate school)
- **Requirements**
 - A, B, or C in 2031
 - Confidence in your lab skills



Being a TA

- You have a good idea how it works by now
 - Lead TA is often the technical expert in a section
 - GTA is primarily there for writing support
 - New UTAs are valued for their ability to field some questions and direct others to the right person
 - You don't need to have all the answers
- So apply on the web site if you are interested
 - You will receive permission to register if selected
 - Don't expect to hear anything until late December