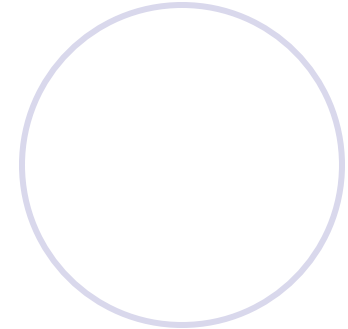
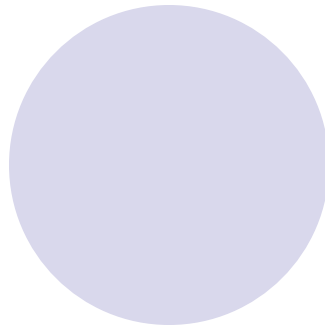
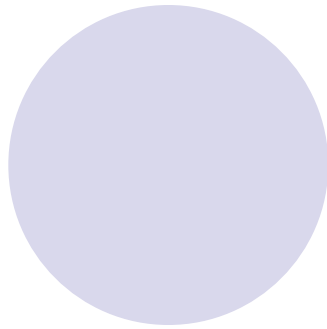


Review for  
Practical Final Exam  
and (later) In-Class Exam



# Announcements



- Practical Exam Monday/Tuesday (June 29-30) IN LAB (your scheduled time)
- Three more weeks of project work, then Final Demos
- Written In-class Exam Friday, July 17 (during lecture period)



# Practical Final exam

- Will be held **IN YOUR REGULAR LAB SESSION**
- No make-ups except in those same severe conditions that the Institute would consider as valid for any other final exam
- There is **NO** exam for this course during finals week
- Approximately 2.5 hours of “practical” exercises (working with lab tools, both hardware and software)
  - You must start on time if you want all the time



# Practical Exam Procedures

- Open book, open notes
  - You'll do better if you don't have to hunt for answers
- TAs cannot assist you with basic skills, setup, etc.
- You cannot access your own home directory, Internet, floppies, or other media (or use ftp, http file transfers)
- Each answer gets checked off by TA
  - Full credit if correct on first checkoff attempt
  - Half credit if correct on second checkoff attempt
- Move on after two attempts
- No requirement to go in order. Plan your own time.



# Practical Exam Content

- Probably about 5-6 numbered problems, some with multiple parts
  - A problem may have multiple parts with some interdependence, but a numbered problem will not depend on a previous one.
- Most emphasize one or more aspects of the design tools (Block Editor, VHDL compiler, Timing Analyzer, Waveform editor, Simulator, Oscilloscope, Logic Analyzer, etc.)
- No need to bring chips or protoboard or wire kit.
- Some exercises require oscilloscope and/or logic analyzer measurements
  - You must connect probes to the expansion header of the UP3 board

# Practical Exam: You Should Know How To ...

- Use Altera's tools, including
  - Schematic entry,
  - VHDL entry,
  - Waveform Editor,
  - Timing Analyzer/Simulation,
  - Pin/device assignments,
  - Compilation, and
  - Programming (downloading)

# Practical Exam: You Should Know How To ...

- Use a part from Altera library
  - understand its help file, etc.
- Find things on the UP3 board
  - Where Cyclone pins go to headers, switches, etc.
  - ByteBlaster connector, VGA connector, etc.
- Download sof files to the UP3 board

# Practical Exam: You Should Know How To ...

- Write/understand VHDL
  - Write the VHDL code to synthesize a given word description or circuit
  - VHDL coding could be “from scratch” on practical final exam

# Practical Exam: You Should Know How To ...

- Work with state machines
  - Generate an ASM chart for a state machine from a word description
  - Generate the VHDL CASE statement to synthesize a state machine from an ASM chart
  - Recognize bugs in implemented VHDL state machines, when compared with the corresponding state diagram
  - Work with state machine examples like simple versions of the train controller

# Practical Exam: You Should Know How To ...

- **Alter SCOMP**
  - Implement new instructions
  - Find bugs
- **Program SCOMP**
  - Write short programs
  - Use SCASM to assemble
  - Verify operation

# Practical Exam: You Should Know How To ...

- Use Oscilloscope

- Use the oscilloscope to perform basic measurements of signals (propagation delay, rise/fall time, duty cycle, period, frequency, etc.)
- Be able to capture a trace that clearly shows these values, with appropriate time scale and voltage scale

- Use Logic Analyzer

- Be able to capture a small number of waveforms, triggering on some event (rising/falling edge) in one of those waveforms
- Compare capture to a simulation or some other prediction of what a circuit should be doing

# How to prepare



- If you understood what you were doing in each lab, and still remember, you are probably prepared
- If you did poorly on a lab, or managed a good grade on something that didn't really make sense, you should consider going through it again
- Exercises will not be the same as labs, but the tasks are similar