Review for Practical Final Exam
Practical Final exam

- Will be held IN YOUR REGULAR LAB SESSION
  - July 8-9 IN LAB (at your scheduled time)
- No make-ups except in those same severe conditions that the Institute would consider as valid for any other final exam
- There is NO exam for this course during finals week
- Exactly 1.5 hours of “practical” exercises (working with lab tools, both hardware and software)
  - You must start on time if you want all the time
Practical Exam Procedures

- Open book, open notes
  - You’ll do better if you don’t have to hunt for answers
- TAs cannot assist you with basic skills, setup, etc.
- You cannot access your own home directory, Internet, flash drives, floppy disks, or other media (and no ftp, http file transfers)
- Each answer gets checked off by TA
  - Full credit if correct on first checkoff attempt
  - Half credit if correct on second checkoff attempt
- Move on after two attempts
- No requirement to go in order. Plan your own time.
Practical Exam Content

- Four numbered problems, some with multiple parts
  - A problem may have multiple parts with some interdependence, but a numbered problem will not depend on a previous one.
- Most problems emphasize one aspect of the design process
  - Design Entry and compilation (Block Editor, VHDL text editor, compiler)
  - Simulation (Waveform editor, Simulator Tool)
  - Implementation and Test (Timing Analyzer, Programmer Tool, Oscilloscope, Logic Analyzer)
- No need to bring chips or protoboard or wire kit.
Practical Exam: Quartus fundamentals

- Be familiar with Quartus tools, including
  - Schematic (Block Diagram) entry,
  - VHDL entry,
  - Waveform Editor/Simulation,
  - Pin Planner (and device assignment),
  - Compilation,
  - Interpreting Compilation Report (incl. Timing Analysis),
  - Programming (downloading)
Practical Exam: Custom devices and DE2 usage

- Be able to use a part from Altera library
  - Something you have not seen before?
  - Create from MegaWizard, where applicable
  - Understand its help information, etc.

- Know features of the DE2 board
  - Where Cyclone pins go to headers, switches, etc.
  - USB-Blaster connector, VGA connector, etc.

- Download precompiled SOF files to the DE2 board, as in Lab 3
Practical Exam: Writing and understanding VHDL

- Be able to write the VHDL code to synthesize a given word description or circuit
- VHDL coding could be “from scratch” on practical final exam
- Or it could be adding small amounts of code to an existing template (possibly something that does not quite work)
Practical Exam: Working with state machines

- Be able to generate the VHDL CASE statement to synthesize a state machine from a UML statechart
- Know how to recognize bugs in implemented VHDL state machines, when compared with the corresponding state diagram
- State machine examples could include simple versions of the train controller
Practical Exam: SCOMP

- Know how to alter SCOMP
  - Implement new instructions
  - Work with I/O devices (old or new)
  - Find bugs

- And how to program SCOMP
  - Write short programs
  - Use SCASM to assemble
  - Verify operation
  - Demonstrate something with the given I/O devices
Practical Exam: Test equipment

- Oscilloscope
  - You must connect probes to the expansion header of the DE2 board, as needed
  - Use the oscilloscope to perform basic measurements of signals (propagation delay, rise/fall time, duty cycle, period, frequency, etc.)
  - Be able to capture a trace that clearly shows these values, with appropriate timescale and voltage scale

- Logic Analyzer
  - Will not be included in the practical exam
How to prepare

- If you understood what you were doing in each lab (and still remember), you are probably prepared.
- If you did poorly on a lab, or managed a good grade on something that didn’t really make sense, you should consider going through it again.
- Exercises will not be the same as labs, but the tasks are similar.
Questions

- Since this review is online, it makes sense to take questions online
- Send email to BOTH Kevin Johnson and Dr. Collins:
  - KJohnson@gatech.edu
  - tom.collins@gatech.edu