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Introduction

This workbook provides supplementary material for the Digital Design Laboratory, supporting ECE2031. The schedule, exercises, and procedures vary from one semester to the next, and this workbook includes all information that is specific to the summer semester of 2013.

The required textbooks for this lab are


In the lecture and elsewhere, these will normally be referred to as the “lab manual” and the “textbook,” respectively. The lab manual is the starting point for each lab exercise, and it refers to sections of the textbook, as needed.

The web site will also be a valuable resource:

http://diglab.ece.gatech.edu

The laboratory is located in room E283 of the Van Leer building. Although “open” hours will be available for general use, all students have an assigned laboratory section that they are expected to attend. During the normal period for each section, prelab quizzes are given, assignments are explained, and written reports are submitted for grading. After the quiz, available extra workstations may be used by students from other sections.

There are 22 computers for student use in the lab. Alongside each computer is a prototyping unit, oscilloscope, logic analyzer, and programmable logic development board, as shown in Figure 1.
The ECE Undergraduate Professional Communication Program

An important part of this course is the ECE Undergraduate Professional Communication Program (UPCP), often called the “Writing Program.” For EE and CmpE majors, this will be the first of several courses in which you are instructed in techniques for presenting technical information. CS majors taking ECE2031 have the same technical communication requirements and get the same advice and consultation on written and oral communication skills. Another valuable resource will be the UPCP web site:

- [http://upcp.ece.gatech.edu](http://upcp.ece.gatech.edu)
Faculty and Staff

With almost 200 students in ECE 2031 during some semesters, it requires a large group of faculty and staff to provide some personal attention to each student.

**Dr. Thomas Collins** ([tom.collins@gatech.edu](mailto:tom.collins@gatech.edu)) is the instructor who presents the lecture each week. He also is the administrator of the lab facilities, and he determines all quiz and exam problems, creates new laboratory exercises, and determines the final grades. Dr. Collins received his Ph.D. from Georgia Tech in 1994 and has an active research career at the Georgia Tech Research Institute in robotics, embedded systems, and high-performance computing. In addition to having taught courses related to this one here at Georgia Tech, he has worked for IBM, Hewlett Packard, and other companies.

Office Location: College of Computing Building, Room 258  
   – detailed instructions at [http://diglab.ece.gatech.edu/tcollins/RIMoffice.html](http://diglab.ece.gatech.edu/tcollins/RIMoffice.html)

Office Hours: Thursday 5:00-6:00 and Friday 4:00-6:00
Telephone: 404.385.2637
(When you arrive at the second floor of the College of Computing building, you will have to call this number to be let in. There is a phone there with preset numbers, or you can use your cell phone.)

**Lecturer Kevin Johnson** ([KJohnson@gatech.edu](mailto:KJohnson@gatech.edu)) is the co-instructor for this course. He is a graduate of Georgia Tech (BSEE, MSEE), and he has been through all aspects of ECE2031 (student, UTA, Lead UTA, and GTA). He plays the lead role in the formulation of the communication-related assignments (reports and oral presentations), sets the requirements for formatting reports, and supervises the grading of these reports through the Graduate Teaching Assistants. He works under the direct supervision of Christina Bourgeois ([christina.bourgeois@ece.gatech.edu](mailto:christina.bourgeois@ece.gatech.edu)). instructor Bourgeois is the coordinator of the Undergraduate Professional Communication Program (UPCP) in ECE. Kevin also serves as the ECE2031 lab administrator. In addition to being able to resolve a variety of lab hardware and software problems, he is a valuable resource for complicated design problems late in the semester.

Office Location: Van Leer Room E276
Telephone: 404.894.2924

The GTAs (Graduate Teaching Assistants) handle the grading of all written reports and exams. A GTA is assigned to each laboratory section and is available during the early part of the section’s scheduled period both for writing-related assistance and general technical help. **Students should always contact their GTA first for any questions about assignment format and grading, because the GTA is the person who will be doing the grading.** In the current semester, some of the more experienced GTAs are doing the grading of major assignments for a new GTA.

The Lead TAs are undergraduates who have been through the course, served at least one semester as a UTA (see below), and were selected based on their technical skills and their instructional abilities. There is one Lead TA assigned to each section, and they run the lab session along with the assigned GTA. During some semesters, especially during summer semester, LTAs also run some of the open hours.
The UTAs are undergraduates who have also been through the course, some as recently as the previous semester. They are familiar with the laboratory exercises, and usually at least two of them will be available at all times that the lab is open. They are usually enrolled as students in ECE 4901 (Special Projects). You, too, can become a UTA, so think about it as the semester progresses.

The key thing to remember is that your Lead TA and your GTA are your primary resources for the personal assistance that the faculty cannot provide to each and every student every week of the semester. Together with the other UTAs, they keep the student-teacher ratio for this course less than 5:1. There are procedures (described below) to get additional attention from the faculty when you need it, though.

### Syllabus and Schedule

The lecture held on Friday of each week is designed to provide information necessary to understand the laboratory assignments for the following week. This includes some review of prerequisite material in the context of the laboratory environment. **No labs are held during the first week of classes, since no lecture will have taken place for students prior to their lab period.**

### Topical Outline:

Laboratory projects will use a PC based CAD Tool environment that supports schematic capture, logic simulation, and VHDL based logic synthesis on FPGAs (Field Programmable Gate Arrays). Discrete logic devices will be used for two designs, but VHDL-based logic synthesis on FPGA-based design boards (with hundreds of thousands of equivalent gates) will be used for more advanced design implementations. The semester will culminate with design projects specified and undertaken by teams of four to five students. Technical writing skills are developed through laboratory reports, project documentation, and an informal presentation.

**Topics:**

- CAD Tools
- Combinational design using multiple methods: discrete logic devices, schematic capture for FPGAs, and VHDL
- Examination of real timing issues on hardware using timing simulation, oscilloscope, and logic analyzer
- State machine specification, design, and simulation
- State machine implementation with multiple methods
- VHDL models of basic gates and logic operations
- Logic synthesis and simulation using VHDL
- VHDL-based simulation and synthesis with programmable logic devices
- Design verification with a logic analyzer
• VHDL models of data storage elements
• ROM and RAM implementations on an FPGA board
• Hardware design of a simple computer with ALU, registers, control unit, memory, instructions, and I/O
• VHDL-based simple computer simulation and implementation on FPGA board
• Machine language and assembly language programming for the simple computer
• Simulation and implementation of programs on the FPGA board
• Final design project problem specification (examples: video game, control application, robot, or contest)
• Hardware and tools available to solve the final design project problem
• Project engineering issues: top-down vs. bottom-up design, hierarchical decomposition, and modularity

In addition to the textbook and lab manual described earlier, you will need to have the following:
• hardware:
  o a wire kit,
  o a chip set, and
  o a protoboard
• USB storage devices as needed to take files to and from the lab and to save data from lab instruments
• your personal GT computer account and GT Active Directory password, which must be activated before the first lab (see the OIT support center if you have never accessed a campus Windows-based computer).

None of the hardware is needed for the first lab, but ALL of it is needed for the second lab. The web site describes sources for all needed items.

You will learn in Labs 1 & 2 that there are different “families” of discrete logic chips (integrated circuits with logic gates in them). These are what are included in your chip set, listed above. At one time, this lab used only the 74LS TTL logic family of logic chips, but now we prefer the 74HCT logic family. Even though the printed manual refers to the 74HCT chips, you may use chips from either family or a mixture of both families – as long as you know what you have and how to use it. 74HC chips are also usable. When the time comes to look up information about your chips in “datasheets,” you must be conscious of the logic family for each chip!

The lab manual provides detailed information about prelab assignments and recommended reading from the textbook. For any given lab, this prelab material should be reviewed as soon as possible, preferably before the corresponding class lecture. Prelab quizzes will be given at the beginning of the lab, and about 15 minutes will normally be allowed. Students who are late will have less time to work on the prelab quiz or may miss it entirely.

There will be one in-class exam, given late in the semester. There will also be an in-lab practical final exam late in the semester. There is no exam during finals week.
Grades are determined according to the following weighting method:

- 30% reports, including
  - lab checkoffs,
  - technical content,
  - writing style,
  - grammar, spelling, and attention to formatting guidelines, and
  - final project demonstration
  - final project presentation
- 25% prelab quizzes
- 20% in-class exam
- 25% practical exam

Note that you can compute your own uncurved grade at any time by applying these weights to the scores you have received to date. Since any curve would be applied only in the last few days of the semester, your uncurved estimate is the best indicator of your grade. Typically, the curve is no more than 1-2 percentage points at each grade cutoff, so it’s usually unrealistic to assume, for example, that an 85 might be an “A.”

An additional factor, the “TA perspective,” is a subjective evaluation of each student’s abilities by the TAs who know them best. This is used to determine the final grade of any student in a borderline situation, which typically applies to between 5% and 15% of the class. It can only pull students up, and will never be used to pull a student down below a grade break. Dr. Collins and Kevin Johnson may also provide input to TA perspective grades.
Laboratory Overview

Most labs consist of

1. Doing prelab exercises and reading assignments prior to the corresponding lab session,
2. showing up on time, turning in any written assignments that are due, and presenting your prelab work for the first lab “checkoff”,
3. taking a prelab quiz,
4. completing the laboratory exercises under the direction of the TAs, getting more checkoffs along the way, and
5. turning in hardcopies of “results” prior to the due date, usually one week after the period where the lab was performed.

All labs have checkoff sheets, which may be found only in a new copy of the lab manual. A TA must verify all steps and check them off. The completed sheet must be turned in at the designated date with the associated results. **Any set of lab results turned in without the ORIGINAL checkoff sheet from the lab manual will not be graded. One or more missing or late checkoffs will result in proportional loss of points. A missing checkoff sheet will result in loss of ALL points.**

Open hours are provided according to the availability of TAs. In general, open hours are not a substitute for the assigned sections, and there is no guarantee that equipment will be available. TAs will limit time as necessary, so being first in the lab does not entitle a student to sole uninterrupted access to a workstation. During open hours, checkoffs are made with no attempt to note late penalties. The TA will note the date and time so that the GTA can determine whether the work was completed on time. **No student is allowed in the lab without a TA.**

Since there are limited open hours, during most regular sections at least two extra workstations will be available under the same terms as during open hours, but only after the prelab quiz is completed.

Each student has personal storage disk space that maps to the “Z” drive. This should be used as a backup, along with personal storage media as required. The CAD software has been known to have errors when compiling files on a network drive. **Errors or not, compilation is 5-10 times SLOWER when you compile files on your Z drive or your desktop (which is also a networked resource).** So, it is wise to copy working files to a local directory, but it is a violation of the honor code to leave files on the local drive or to make any attempt to recover files created by other students.
Scheduled Activities

The activities for each week of the semester are given in a schedule on the course web site:

http://diglab.ece.gatech.edu/downloads/Summer13Calendar.pdf

Open hours will depend on TA availability, but will always include free workstations in regular sections, as described earlier.

See the web site at http://diglab.ece.gatech.edu/lab.html for a detailed HOURLY lab schedule for each week, including the section times, TA assignments, and exact hours of Open Hours. That page defaults to the GTA assignments, but UTA and LTA assignments are linked there, too.
Lab Procedures

Late Policies

All assignments are due at the beginning of your assigned lab time (as you walk in
the door) on the date specified on the schedule above. **Late assignments will not be accepted**
(except under extenuating circumstances*). For full credit, all prelab exercises must be completed before coming to lab. The first 15 minutes of lab will
be structured as follows: turn in any assignments due for the day, take the quiz, and
obtain prelab checkoffs. Students are expected to abide by the policies and
procedures outlined below in the order in which they appear:

1. **Turn in all assignments as you walk in the door.** Late assignments will not be accepted. Incomplete assignments can be turned in for partial credit, but missed checkoffs incur significant penalties.

2. **Take quiz.** If you are not prepared to turn in any assignments that are due, simply inform your GTA. Only then can you take the quiz.

3. **Obtain prelab checkoff.** For full credit, all prelabs must be completed prior to your scheduled lab time. You may continue to work on prelab exercises during class, since you may need some hardcopy to turn in as part of your results, but you will lose some points for the late checkoff(s). Students should have their prelab exercises out and be ready for a checkoff as soon as they are seated. TAs may do the prelab checkoffs during the prelab quiz, or immediately afterward.

There is no printer in the lab. All assignments (and any accompanying materials)
must be printed, filled out, and stapled prior to your scheduled lab time. This rule is
necessary to prevent EVERYONE from trying to print nearby at the last minute. It is
good practice to have everything printed hours ahead of time, or preferably the night
before, especially since there is no printer in the lab.

**Nothing will be accepted after the first twenty minutes** (e.g., after 3:25 for a lab
that starts at 3:05). No prelab quizzes, no prelab checkoffs, and no assignments
due from previous labs.

* Extenuating Circumstances

Extenuating circumstances that prevent a timely submittal of an assignment MUST either
a) be discussed with Kevin Johnson at least **24 hours** prior to the due date, or
b) be of a nature that under Institute policies would be unquestionably accepted by the Office of the Dean of Students
(including a death in the family, serious injury, or illness). The Office of the Dean of Students does not necessarily
have to be involved, but they could be involved in cases as needed.

Students must be able to provide appropriate documentation verifying the extenuating circumstances that prevented a
timely submittal of the assignment. Schedule conflicts, technical difficulties (corrupted disks, printer problems,
crashing computers), and procrastination will not be treated as extenuating circumstances. Please plan accordingly,
saving all files repeatedly and backing up all work periodically.
Grade Disputes

All students have the right to ask questions about the grades they receive on assignments. Students who wish to discuss their grade must follow the procedures outlined below:

1. Make an appointment where you can discuss the grade with your GTA outside of the lab and in private.
2. If you still have questions or concerns about your grade for a writing assignment, send an email to Kevin Johnson that clearly and concisely explains the problem. For concerns about a quiz or exam that remain unresolved after discussions with your GTA, send an email to Dr. Collins or visit him during office hours.
3. Sometimes an email response from Kevin or Dr. Collins may be enough to solve the problem, but they may request that you make an appointment to discuss the grade, or you may feel it necessary to request an appointment yourself.
4. When Kevin or Dr. Collins become involved in re-grading an assignment, the entire assignment will be reviewed, not just the area questioned by the student. Understand that your score could go up or down upon review.

Communication

From time to time, last-minute announcements will be necessary. Students are responsible for reading their email and checking the website. Often, email is not delivered because students run out of space in their OIT accounts or redirect mail to another address with limited storage space. Partly for this reason, the websites are preferred over email as a means of communication, but note that all class email is sent to the T-Square address, so it will remain available in the T-Square email archive. Check both websites (diglab.ece.gatech.edu and upcp.ece.gatech.edu) and the T-Square email archive often, at least on the days immediately preceding a due date or exam!

The ECE2031 faculty members have no direct control over the class mailing lists, because they originate from the T-Square server. T-Square support staff members are the only people who can help you with mailing lists. If you are convinced that other students in class are getting class-related email that you are not receiving yourself, then do the following:

1. Get someone to forward the message in question to you,
2. Make sure that it was directed to the whole class (i.e., that it was not sent by a specific TA just to their section),
3. Go to the “Help” section of T-Square. Contact the support staff and forward the message you got in step 1, and explain that you are in ECE2031 and you believe that you should have received that message.

T-Square forums may be enabled for the class as needed, especially during the final project. Acceptable questions include clarification of assignments, tips and tricks for
using the laboratory tools, etc. **Seeking direct answers to fundamental lab exercises is inappropriate and considered to be a violation of the honor code, as is answering such questions.** TAs who monitor the forums will ensure that Dr. Collins is made aware of questions that cannot be answered by anyone but faculty.

If an email question is directed to faculty, and it is determined that the question is both valid and general in nature, the answer will probably be given to the entire class, with the name of the original sender removed.

**Penalty points**

Penalty points can be assigned to students for the following reasons:

- Leaving trash
- Unauthorized tampering with laboratory equipment (possibly severe penalties or fines)

Attendance and time spent in the lab affects the TA perspective, the subjective evaluation mentioned earlier that can make the difference in the letter grade of a borderline student.

**Missed Work**

One quiz can be dropped. If only one is missed, that’s the one that is dropped. If more quizzes are missed, you must have valid documentation for excuse on ALL missed ones, and you are allowed to make up all but the first one (by some means to be determined by Dr. Collins). If no quizzes are missed, the lowest one is dropped automatically. Here it is one more time, because some students always miss this: **You get to drop a low quiz score, but if you use your drop for an unexcused absence, you CANNOT get it back, even if your next absence is excused.**

**Honor Code**

All aspects of the Georgia Tech Honor Code apply and will not be repeated here. Some key points follow.

Do not plagiarize or engage in academic misconduct. Plagiarism is the act of using someone else’s words, ideas, or organizational patterns without giving credit to the source. It constitutes a serious offense and is a violation of the Academic Honor Code. Georgia Tech and the School of ECE define plagiarism as “Submission of material that is wholly or substantially identical to that created or published by another person or persons, without credit notations indicating authorship” (Section XVII. C. Academic Misconduct, General Catalog).

Do not copy or cut-and-paste from any websites, textbooks, lab manuals, etc. simply to create material for your reports. Citing other sources can be a valuable way to bolster your conclusions, and direct quotes can be particularly relevant or entertaining, but should you find it necessary to consult these types of resources, you must cite your source(s). **Refer to the Mayfield Handbook for proper documentation of sources (IEEE formatting only).** Additionally, be aware that inappropriate collaboration is considered a violation of the Honor Code and will be treated as academic misconduct. Students may, of course, discuss assignments in general.
terms with one another, but all work should be generated individually (except for those labs specified as group or team projects). Likewise, students may receive assistance on lab reports from the course instructor, lab instructors, or writing consultants. However, students are expected to write their own reports and do their own work. Copying or allowing peers to copy or paraphrase all or portions of lab reports is considered plagiarism and academic misconduct. All instances of academic misconduct will be immediately reported to the Dean of Students.

**Under no conditions is it ever acceptable to copy even the smallest fragments of another student’s work without specifically citing the source.** If you cite another student as the source, it may impact the grade (depending on whether that was considered to be appropriate), but at least you will not face plagiarism charges under the Honor Code.

Do not attempt to gain special access to TAs that you know personally, or to gain access to the lab outside of the time made available to your section or to the class as a whole. (It is allowable for an LTA or a GTA to conduct special tutorial sessions for an entire section, either in the lab or elsewhere.)

Additional requirements for ECE2031 include the following:

- Students must keep electronic copies of all material that is submitted for grading.
- Students must never leave files on disks in the lab, nor leave results accessible to other students. Attempts to recover files or other intellectual property of other students are also forbidden.

The material formerly included here as “Guidelines for Writing and Formatting ECE2031 Documents” has been moved to the UPCP site.